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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,406	01/26/2004	Darrell Rinerson	UNTYP030	2199

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,406	RINERSON ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2004 and 16 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/09/2005 has been entered.

2. Applicant's arguments with respect to claims 1-2 and 4-48 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter that the applicant regards as his invention.

3. Claims 1-2 and 4-48 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Each of **claims 1 and 25** recites: "high temperature" which is not clear. Since Applicant has not clearly defined "high temperature" in the specification, it is not clear how high is high in the claim. For example, 200 °C is considered high by Ahn et al. (U.S. Patent 6,297,038, column

6, lines 10-20), while Nomoto et al. considered 800 – 1000 °C high (U.S. Patent Application Publication 20010044185, paragraph [0004]).

Each of **claims 1, 25, 33, and 44** recites a layered material that is stable at a certain temperature and another layered material that is not stable at the certain temperature, which are not clear. As noted above, since the certain temperature is not distinctly pointed out, the limitation as a whole is not distinct. Furthermore, the very limitation "stable" is also not distinct. For example, melting point of the popular conductive material aluminum is 660 °C and that of copper is 1083 °C (the two materials that Applicant considered stable at the undefined temperature as cited in, for example, claim 6. Exactly at what temperature should every artisan in the semiconductor art unanimously consider aluminum or copper "stable"?

Claim 33 recites: "wherein the memory plugs have at least one layer that requires the minimum temperature for fabrication greater than 450 °C", which is not clear. First, the metes and bounds of the limitation is not established: how would an artisan discern products that are formed at a minimum temperature for fabrication greater than 450 °C from similar products that are not formed at a minimum temperature for fabrication greater than 450 °C? Secondly, it has well been established that a processing conduction in a product claim is considered a non-limitation (MPEP 2112.01 and MPEP 2113).

Nevertheless, for examination purposes, the certain temperature is considered at least 450 °C and the layered materials that are "stable" at 450 °C are refractory metals, such as tungsten, and the layered materials that are not "stable" at 450 °C are aluminum or copper.

Claims 2, 5-24, 26-32, 34-43, and 45-48 respectively depend from rejected claims 1, 25, 33, and 44 and include all limitations of claims 1, 25, 33, and 44 thereby rendering these claims indefinite.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. **Claims 1-2, 5-9, 24-28, 33-37, and 45,** insofar as in compliance with the 112 rejection noted above, are rejected under 35 U.S.C. 102(e) as being anticipated by Ishii U.S. Patent Application Publication 20010017798 (the '798 reference).

Referring to **claims 1-2, 5-9, 25-28, and 33-37**, the reference discloses a re-writeable cross point memory comprising:

a substrate (Fig. 1, generally defined by elements 6, 7, 8, 9, 10, 100) having a deposition face, the substrate including active circuitry (generally indicated as "transistors", paragraph [0036]) having multiple layers of conductive paths (100, 10), the conductive paths being formed of a high melting point material such as tungsten and tantalum (paragraph [0043]); and

a memory array (MRAM, indicated generally at the portion above the deposition face of the substrate, Fig. 1; and disclosed in paragraph [0034]) positioned above the deposition face and over the active circuitry and including:

a plurality of memory cellular plugs (the limitation "formed using high temperature processing" is taken to be a product-by-process limitation and considered non-limitation in a product claim (MPEP 2112.01 and MPEP 2113));

a bottom (first) refractory metal that has a melting point above 450 °C, the bottom refractory metal layer positioned parallel to the deposition face of the substrate and patterned into (x-direction) bottom conductive array lines (note that Fig. 1 does not depict bottom conductive array lines because Fig. 1 describes a thin-film transistor (TFT) memory cell; for a resistive magnetoresistive random access memory (MRAM), there must be patterned bottom conductive array lines – see, for example, the '821 reference, cited in a previous office action; as for the limitation "refractory metal", the '798 teaches that metal lines underneath memory elements shall be refractory metals, paragraph [0043]) ;

a top (second) metal layer (5) formed of aluminum or copper (paragraph 0043], which is not a refractory metal) and positioned parallel to the deposition face of the substrate, patterned into (y-direction) top conductive array lines (Figs. 1 and 7) such that a memory cell may be at least partially defined by the intersection of a bottom conductive array line and a top conductive array line, the memory cell capable of being programmed by application of voltages on the bottom conductive array line and the top conductive array line, as is known in the resistive memory MRAM art and in the resistive non-MRAM memory art.

Referring to **claims 24 and 45**, the reference further discloses that the number of arrays could be larger than two (paragraph [0010]) and that only the topmost metal layer is not a refractory metal layer (i.e., aluminum, paragraph [0043]).

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. **Claim 44,** insofar as in compliance with the 112 rejection noted above, is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii U.S. Patent Application Publication

20010017798 (the '798 reference) and further in view of Ignatiev et al. U.S. Patent 6,473,332 (the '332 reference, cited in a previous office action). **Claims 4, 39-42, and 46,** insofar as in compliance with the 112 rejection noted above, is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii U.S. Patent Application Publication 20010017798 (the '798 reference) as applied to claims 1-2, 5-9, 24-28, 33-37, and 45 above, and further in view of the '332 reference.

The '798 reference discloses a re-writeable cross point memory as claimed and as detailed above, but the reference's memory is a resistive MRAM (magnetoresistive) memory, therefore the memory cells do not include a conductive metal oxide or a crystalline material. Furthermore, at the time the invention was made, it did not appear that MRAM was formed at at least 450 °C (in reference to claim 44).

The '332 reference, in also disclosing a memory device, teaches that a resistive memory device including a conductive metal oxide, as detailed in a previous office action, is a much better memory device than an MRAM (column 2, line 21: "In the case of the magnetoresistive oxide devices, magnetic switching fields are generally high and temperatures of operation are very low..... Thus, there is a need in the art for new resistive memory systems that are capable of storing data in a non-volatile and multi-valued manner using traditional read voltages and relatively low write voltage pulses of relatively short to very short duration and good fatigue resistance properties"; and the new resistive memory is the memory including a conductive metal oxide, as detailed in a previous office action and detailed throughout the specification of the '332 reference).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '332 reference's resistive memory device such that in place of the MRAM cells are memory cells with conductive metal oxides. One would have been motivated to make such a change in view of the teachings in Ignatiev the '332 reference that such a modification results in a much better memory device.

As for the limitation "at least 450 °C", it shall be apparent that the metal oxide of the modified resistive memory device is formed at at least 450 °C.

As for the materials for the electrodes cited in claims 39-42, the '332 discloses such materials and as detailed in a previous office action.

6. **Claims 10 and 47,** insofar as in compliance with the 112 rejection noted above, is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii U.S. Patent Application Publication 20010017798 (the '798 reference) and further in view of Ignatiev et al. U.S. Patent 6,473,332 (the '332 reference, cited in a previous office action) as applied for claims 1 and 46 above, and further in view of Hsu et al. U.S. Patent Application Publication 20040235247 (the '247 reference, cited in a previous office action).

The '798 reference's device, modified in view of Ignatiev as detailed above so as to have a better memory device (the '798/332 device), still lacks the limitation "two conductive metal oxide layers that are not identical to each other" as claimed.

Hsu, in also disclosing a resistive memory device, teaches that a resistive memory device having two conductive metal oxide layers that are not identical to each other insures reliable memory properties (paragraphs [0022] to [0025]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '798/332 device such that the memory cells includes two conductive metal oxide layers that are not identical to each other. One would have been motivated to make such a change in view of the teachings in Hsu that such a change results in reliable memory properties.

7. **Claims 11-21,** insofar as in compliance with the 112 rejection noted above, is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii U.S. Patent Application Publication 20010017798 (the '798 reference), in view of Ignatiev et al. U.S. Patent 6,473,332 (the '332 reference, cited in a previous office action), further in view of Hsu et al. U.S. Patent Application Publication 20040235247 (the '247 reference, cited in a previous office action) as applied above for claim 10, and further in view of Slaughter et al. U.S. Patent 6,544,801 (the '801 reference, cited in a previous office action). **Claims 22-23, 29-32, and 38** insofar as in compliance with the 112 rejection noted above, is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii U.S. Patent Application Publication 20010017798 (the '798 reference) as applied above for claims 1, 25, and 33, and further in view of Slaughter et al. U.S. Patent 6,544,801 (the '801 reference).

Referring to **claims 11, 23, and 29**, the respective references discloses a memory device as claimed and as detailed above for claims 1, 10, and 25 including the bottom electrode, but fails to teach that the bottom electrode further includes a barrier layer as claimed.

However, at the time the invention was made, Slaughter discloses a memory system including a memory cell 50 comprising a bottom electrode structure 54 having an electrode including a metal layer 72 and a diffusion barrier layer 74 so as to provide a diffusion barrier preventing diffusion of undesirable materials onto underlying, previously formed layers.

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the electrode layer of the respective references such that it includes a barrier layer. One would have been motivated to make such a change because Slaughter teaches

that a memory system including a memory cell comprising a bottom electrode structure having an electrode including a metal layer 72 and a diffusion barrier layer 74 provides a diffusion barrier preventing diffusion of undesirable materials, just as the label suggests.

The various materials and labels recited in **claims 12-22, 30-33** for the electrode including the barrier/buffer/adhesion layer, are known and available to one of ordinary skill in the art, and as detailed in the '332 reference.

8. **Claims 43 and 48,** insofar as in compliance with the 112 rejection noted above, is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii U.S. Patent Application Publication 20010017798 (the '798 reference), and further in view of Monsma et al. U.S. Patent 6,331,944 ('the '944 reference, cited in a previous office action).

The '798 reference discloses a memory device as claimed and as detailed above for claims 1 and 33 including the memory plugs (MRAM), but fails to teach that each of the memory plugs includes a non-ohmic device as claimed.

However, at the time the invention was made, Monsma teaches that a simple steering device, such as a non-ohmic diode device, in series with a memory cell so as to obtain a simple structure with only two terminals per cell and which is easy to fabricate (Figs. 1-2 and column 3, lines 3-28).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the memory plug such that it includes a non-ohmic device. One would have been motivated to make such a change because Monsma teaches that a memory

system including a memory plug having a non-ohmic diode device forms a simple structure with only two terminals per cell and simple fabrication.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
August 19, 2005